IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ian B. McPherson et a.
Serial No. 10/808,724
Filed: 3/25/2004
For: **SYSTEM AND METHOD FOR MEASURING ROUND TRIP DELAY OF VOICE PACKETS IN A TELEPHONE SYSTEM**

Examiner: Raj K. Jain
Art Unit: 2472

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

An **APPEAL BRIEF** is filed herewith. Appellant encloses a payment in the amount of $540.00 as required by 37 C.F.R. § 41.20(b)(2). If any additional fees are required in association with this appeal brief, the Director is hereby authorized to charge them to Deposit Account No. 50-1732, and consider this a petition therefor.

APPEAL BRIEF

(1) REAL PARTY IN INTEREST

The real party in interest is the assignee of record, i.e., Avaya, Inc. of 211 Mount Airy Road, Basking Ridge, New Jersey 07920.

(2) RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences to the best of Appellant's knowledge.

(3) STATUS OF CLAIMS

Claims 1-36 were previously cancelled.

Claims 37-58 were rejected with the rejection made final on January 7, 2010.

Claims 37-58 are pending and are the subject of this appeal.

(4) STATUS OF AMENDMENTS

All amendments have been entered to the best of Appellant's knowledge. No amendments have been made since the final office action mailed January 7, 2010.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

In the following summary, Appellant has noted where in the Specification certain subject matter exists. Appellant wishes to point out that these citations are for demonstrative purposes only and that the Specification may include additional discussion of the various elements, citations to which are not pointed out below. Thus, the noted citations are in no way intended to limit the scope of the pending claims.

Independent claim 37 recites a network device (e.g., Figure 1, elements 100, 110, 120, and 130) for use in a network (e.g., Figure 1, element 150) transmitting packets (e.g., Specification p. 5, ll. 14-15), the device comprising:

a timer (e.g., Figure 4, element 440; see also, e.g., Specification p.7, ll. 12-15);

a processor (e.g., Figure 3, elements 304 and 314) operable for setting a transmit bit in an outgoing packet to a network (e.g., Figure 4, elements 400 and 450; see also, e.g., Figure 5, step

530; see also, e.g., Specification p. 8, ll. 15-16) and starting the timer when the transmit bit is set (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16) and for reading a receive bit in a received packet (e.g., Figure 7, step 720; see also, e.g., Specification p. 9, ll. 12-15) from the network and stopping the timer when the receive bit is read (e.g., Figure 7, step 740; see also, e.g., Specification p. 9, ll. 12-15) and for monitoring a delay time of the network (e.g., Figure 7, step 750; see also, e.g., Specification p. 9, ll. 12-15).

Dependent claim 39 recites the network device in accordance with claim 37 wherein the processor is further operable for reading a set transmit bit in the received packet (e.g., Figure 6, step 620; see also Specification p. 9, ll. 1-2) and for setting a receive bit in another outgoing packet (e.g., Figure 6, step 650; see also, e.g., Specification p. 9, ll. 3-5) in response to reading the set transmit bit in the received packet (e.g., Figure 6, steps 630, 640; see also Specification p. 9, ll. 3-5).

Dependent claim 41 recites the network device in accordance with claim 37 further comprising:

a round trip register (e.g., Figure 4, element 495) operable for receiving a value from the timer (e.g. Figure 7, step 760; see also, e.g., Specification p. 9, ll. 16-19).

Dependent claim 42 recites the network device in accordance with claim 41 wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value (e.g. Figure 7, step 770; see also, e.g., Specification p. 9, ll. 18-20) and sending an indication to a user when the value in the round trip data register is greater than the predetermined value (e.g. Figure 7, step 780; see also, e.g., Specification p. 9, ll. 21-22).

Independent claim 43 recites a device (e.g., Figure 1, elements 100, 110, 120, and 130) for use in a network (e.g., Figure 1, element 150) transmitting packets (e.g., Specification p. 5, ll. 14-15), the device comprising:

a timer (e.g., Figure 4, element 440; see also, e.g., Specification p.7, ll. 12-15);

a transmitting state machine (e.g., Figure 4, elements 410 and 460) operable for setting a transmit bit in an outgoing packet (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll.

15-16) and starting the timer when the transmit bit is set (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16); and

a receiving state machine (e.g., Figure 4, elements 420 and 480) operable for reading a receive bit in a received packet (e.g., Figure 7, step 720; see also, e.g., Specification p. 9, ll. 12-15) and stopping the timer when the receive bit is read (e.g., Figure 7, step 740; see also, e.g., Specification p. 9, ll. 12-15).

Dependent claim 45 recites the device in accordance with claim 43 wherein the receiving state machine is further operable for reading a set transmit bit in the received packet (e.g., Figure 6, step 620; see also Specification p. 9, ll. 1-2) and for setting a receive bit in another outgoing packet (e.g., Figure 6, step 650; see also, e.g., Specification p. 9, ll. 3-5) in response to reading the set transmit bit in the received packet (e.g., Figure 6, steps 630, 640; see also Specification p. 9, ll. 3-5).

Dependent claim 47 recites the device in accordance with claim 43 further comprising:

a round trip register (e.g., Figure 4, element 495) operable for receiving a value from the timer (e.g. Figure 7, step 760; see also, e.g., Specification p. 9, ll. 16-19).

Dependent claim 48 recites the device in accordance with claim 47 further comprising a processing means operable for comparing the value in the round trip data register to a predetermined value (e.g. Figure 7, step 770; see also, e.g., Specification p. 9, ll. 18-20) and sending an indication to a user when the value in the round trip data register is greater than the predetermined value (e.g. Figure 7, step 780; see also, e.g., Specification p. 9, ll. 21-22).

Independent claim 49 recites a system (see, e.g., system depicted in Figure 1) for use in timing the transmission of voice packets (e.g., Figure 2, element 200; see also, e.g., Specification p. 5, l. 22 – p. 6, l. 3) through a network (e.g., Figure 1, element 150), the system comprising:

a timer (e.g., Figure 4, element 440; see also, e.g., Specification p.7, ll. 12-15);

a processor (see, e.g., Figure 3, elements 304 and 314) operable for constructing an outgoing first voice packet to a network (see, e.g., Figure 5, step 520; see also, e.g., Specification p. 8, ll. 14-15) for setting a transmit bit in the outgoing first voice packet (e.g.,

Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16) to the network (e.g., Figure 1, element 150), and for starting the timer when the transmit bit is set (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16), and for monitoring a delay time of the network (e.g., Figure 7, step 750; see also, e.g., Specification p. 9, ll. 12-15).

Dependent claim 50 recites the system in accordance with claim 49 further comprising:

an interface (e.g., Figure 3, elements 308, 318) coupled to the processor, the interface operable for coupling the system to the network (e.g., Specification p. 7, ll. 1-2) and for transmitting the outgoing first voice packet (e.g., Figure 5, step 560; see also, e.g., Specification p. 8, ll. 17-18).

Dependent claim 51 recites the system in accordance with claim 50 wherein the interface is operable for receiving a second voice packet (e.g., Figure 7, step 710; see also, e.g., Specification p. 9, l. 12), and the processor is operable for checking the second voice packet to determine if a receive bit is set (e.g., Figure 7, step 720; see also, e.g., Specification p. 9, ll. 12-13) and stopping the timer if the receive bit is set (e.g., Figure 7, step 740; see also, e.g., Specification p. 9, ll. 13-14).

Dependent claim 52 recites the system in accordance with claim 51 further comprising:

a round trip data register (e.g., Figure 4, element 495) operable for receiving a value from the timer (e.g. Figure 7, step 760; see also, e.g., Specification p. 9, ll. 16-19).

Dependent claim 53 recites the system in accordance with claim 52 wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value (e.g., Figure 7, step 770; see also, e.g., Specification p. 9, ll. 18-20) and sending an indication to a user when the value in the round trip data register is greater than the predetermined value (e.g., Figure 7, step 780; see also, e.g., Specification p. 9, ll. 21-22).

Dependent claim 54 recites the system in accordance with claim 49 wherein the processor is further operable for receiving a second voice packet (e.g., Figure 6, step 610; see also Specification p. 9, ll. 1-2) and checking the second voice packet to determine if the transmit bit is

set (e.g., Figure 6, step 650; see also, e.g., Specification p. 9, ll. 3-5), and further operable for constructing an outgoing third voice packet (Specification, p. 9, ll. 9-10) and setting a receive bit in the outgoing third voice packet if the transmit bit is set in the received second voice packet (e.g., Figure 6, steps 630, 650; see also Specification p. 9, ll. 3-5).

Independent claim 55 recites a network device (e.g., Figure 1, elements 100, 110, 120, and 130) for use in a network (e.g., Figure 1, element 150) transmitting packets (e.g., Specification p. 5, ll. 14-15), the network device comprising:

a link (e.g., Figure 1, elements 122, 125, 132, 135, 300, and 310) for communicating with external devices over the network (e.g., Figure 1, elements 100, 110, 120, and 130; see also, e.g., Specification p. 5, ll. 10-11), the link comprising,

an interface (e.g., Figures 3 and 4, elements 308, 318) operable for coupling the link to the network and for transmitting and receiving packets (e.g., Specification p. 5, l. 22 – p. 6, l. 3; see also, e.g., Specification p. 6, l. 20 – p. 7, l. 8);

a timer (e.g., Figure 4, element 440; see also, e.g., Specification p.7, ll. 12-15); and

a processor (e.g., Figure 3, elements 304 and 314) coupled to the interface (e.g., Figure 3; see also, e.g., Specification p. 6, l. 20 - p.7, l. 5), the processor operable for setting a transmit bit in an outgoing packet to the network (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16), and starting the timer when the transmit bit is set (e.g., Figure 5, step 530; see also, e.g., Specification p. 8, ll. 15-16), and for reading a receive bit in a received packet from the network (e.g., Figure 7, step 720; see also, e.g., Specification p. 9, ll. 12-15), and stopping the timer when the receive bit is read (e.g., Figure 7, step 740; see also, e.g., Specification p. 9, ll. 12-15), and for monitoring a delay time of the network (e.g., Figure 7, step 750; see also, e.g., Specification p. 9, ll. 12-15).

Claim 56 recites the network device in accordance with claim 55 wherein the processor is further operable for reading a set transmit bit in the received packet (e.g., Figure 6, step 650; see also, e.g., Specification p. 9, ll. 3-5) and setting a receive bit in another outgoing packet (e.g., Figure 6, step 650; see also Specification p. 9, ll. 4-5) in response to reading the set transmit bit in the received packet (e.g., Figure 6, steps 630, 640; see also Specification p. 9, ll. 3-5).

Claim 58 recites the network device in accordance with claim 37 further comprising:

a round trip register (e.g., Figure 4, element 495) operable for receiving a value from the timer (e.g., Figure 7, step 760; see also, e.g., Specification p. 9, ll. 16-19);

wherein the outgoing packet and the received packet are voice packets (e.g., Specification, p. 8, ll. 12-15, p. 9, ll. 10-12); and

wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value (e.g., Figure 7, step 770; see also, e.g., Specification p. 9, ll. 18-20) and sending an indication to a user when the value in the round trip data register is greater than the predetermined value (e.g., Figure 7, step 780; see also, e.g., Specification p. 9, ll. 21-22).

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 37-58 were properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,322,793 to Andersson et al. (hereinafter "Andersson") in view of U.S. Patent No. 5,633,861 to Hanson et al. (hereinafter "Hanson").

(7) ARGUMENT

A. Introduction

As an example, claim 37 is directed to "a network device for use in a network transmitting packets." The "network device" is operable to "monitor[ing] a delay time of the network." In this regard, the "network device" includes a "processor operable for setting a transmit bit in an outgoing packet to a network." The "processor" is further operable to "start[ing] a timer when the transmit bit is set." The "processor" is operable "for reading a receive bit in a received packet from the network and stopping the timer when the receive bit is read." The "processor" can "monitor[ing] a delay time of the network" using the delay between the start of the timer and receive of the receive bit from a received packet.

The Patent Office has not shown where all the elements of the pending claims are shown in the prior art with sufficient particularity to sustain an obviousness rejection. In particular, the Patent Office has not established how the prior art discloses or suggest a device that is operable to set a transmit bit in an outgoing packet to a network, and **start a timer when the transmit bit is set**. Further, the Patent Office has not shown how the prior art discloses or suggest a device

that is operable **stop the timer when the receive bit is read** to determine delay time of the network. As such, Appellant requests that the Board reverse the Examiner and instruct the Examiner to allow the claims for these reasons along with the reasons noted below.

B. Summary of References

1. U.S. Patent No. 4,322,793 to Andersson et al.

Andersson is related to a data communication interface for a CPU-based architecture and is not related to network packet communications. Andersson discloses a communications controller integrated into a central processing unit (CPU) that connects a low speed programmable I/O bus (PIO bus) to a high speed integrated channel bus via an interface utilizing an integrated communications adapter (ICA) bus adapter. Andersson, col. 2, ll. 20-25. The function of the ICA bus adapter is to support the PIO-bus and allow the common communications adapter (CCA) to link to the microcode on the integrated communications controller (ICC) of the CPU via traps and sense and control commands. Andersson, col. 4, ll. 48-52. Despite the assertions made by the Patent Office, the CCA timer in Andersson is not started when a transmit bit is set, and is not stopped when a receive bit is read. Rather the time out intervals cited by the Patent Office are ***predetermined*** amounts of time counted down by the CCA timer as a time-out mechanism. Andersson, col. 13, ll. 40-41; col. 14, ll. 12-15; col. 14, ll. 25-27; col. 14, ll. 34-40; col. 14, ll. 44-47; col. 15, l. 5 – col. 16, l. 1; col. 17, ll. 30-32.

During asynchronous transmission and reception, the CCA in Andersson, through an ICA Start/Stop Line Control Facility, activates interrupts so that the low-speed PIO bus can request a service from the ICC on the CPU. Andersson, col. 13, ll. 54-59. These interrupts may set sense and control registers within the ICA bus adapter and determine the functionality of the traps and sense and control commands. Andersson col. 4, ll. 48-54. A handling module in the ICA Start/Stop Line Control Facility examines the registers of the CCA and determines when to start and stop the transmission and reception of bytes. Andersson, col. 14, l. 61 – col. 16, l. 5. The system of Andersson checks if certain events or conditions related to the Start/Stop Commands have occurred by having the CCA timer count down to a *predetermined time out interval* and experience a "time out." Andersson, col. 14, ll. 12-15; col. 14, ll. 25-27; col. 14, ll. 34-40; col. 14, ll. 44-47; col. 15, l. 5 – col. 16, l. 1. The CCA timer is not started when a transmit bit is set

or when a receive bit is read as alleged by the Patent Office, but rather simply counts down *predetermined amounts of time*.

2. U.S. Patent No. 5,633,861 to Hanson et al.

Hanson discloses a packet-based communication network for exchanging data packets between different nodes within the network. Hanson, col. 2, ll. 37-46. Otherwise, Hanson does not disclose any of the features of the claims. The Patent Office simply cites Hanson, because the Patent Office believes that the communications network in Hanson can be combined with teachings of Andersson to monitor a delay time on the packet-based communications network. Office Action of January 7, 2010, p. 3.

C. Legal Standards

1. For Establishing Obviousness

Section 103(a) of the Patent Act provides the statutory basis for an obviousness rejection and reads as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Courts have interpreted 35 U.S.C. § 103(a) as a question of law based on underlying facts. As the Federal Circuit stated:

> Obviousness is ultimately a determination of law based on underlying determinations of fact. These underlying factual determinations include: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) the extent of any proffered objective indicia of nonobviousness.

Monarch Knitting Mach. Corp. v. Sulzer Morat GmBH, 45 U.S.P.Q.2d (BNA) 1977, 1981 (Fed. Cir. 1998) (internal citations omitted).

Once the scope of the prior art is ascertained, the content of the prior art must be properly combined. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demand known to the design community or present in the marketplace; and

the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit. *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex, Inc.*, 550 U.S. 398, 418, 82 U.S.P.Q.2d (BNA) 1385, 1396 (2007).

While the Patent Office is entitled to give claim terms their broadest reasonable interpretation, this interpretation is limited by a number of factors. First, the interpretation must be consistent with the specification. *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000) M.P.E.P. § 2111. Second, the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. Finally, the interpretation must be reasonable. *In re Cortright*, 165 F.3d 1353, 1359 (Fed. Cir. 1999) M.P.E.P. § 2111. This means that the words of the claim must be given their plain meaning unless the Appellant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989).

When rejecting a claim under § 103, the Patent Office must either show that the prior art references teach or suggest all limitations of the claim or explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art. *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 418, 82 U.S.P.Q.2d (BNA) 1385, 1396 (2007). To establish *prima facie* obviousness, the Patent Office must show where each and every element of the claim is taught or suggested in the combination of references. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. (BNA) 580 (CCPA 1974). The gap between the prior art and the claimed invention may not be "so great as to render the [claim] nonobvious to one reasonably skilled in the art." *Dann v. Johnston*, 425 U.S. 219, 230, 189 U.S.P.Q. (BNA) 257, 261 (1976). If a claim element is missing after the combination is made, then the combination does not render obvious the claimed invention, and the claims are allowable. If the PTO fails to meet this burden, then Appellant is entitled to the patent. *In re Glaug,* 283 F.3d 1335, 1338 (Fed. Cir. 2002).

D. Claims 37-58 Are Patentable Over Andersson in View of Hanson

Claims 37-58 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Andersson in view of Hanson. Appellant respectfully asserts that the Patent Office's rejection of the claims is incorrect and requests that the Board reverse the rejection of the claims under 35 U.S.C. §103(a).

1. None of the Cited References Either Alone or in Combination Discloses a Processor Operable For Starting a Timer When A Transmit Bit is Set, Reading a Receive Bit in a Received Packet From the Network, and Stopping the Timer When the Receive Bit is Read in Accordance with Claim 37

When rejecting a claim under 35 U.S.C. §103, the Patent Office must either show that the prior art references teach or suggest all limitations of the claim or explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007). Here, the Patent Office has failed to show where each and every limitation of the claims is taught or suggested by the prior art. Further, for those limitations of the claims that are not taught or suggested by the prior art, the Patent Office has failed to explain why those limitations would have been obvious to one of ordinary skill in the art.

Claim 37 is directed to a network device for "monitoring a delay time" of a network. To do this, the network device of claim 37 includes a processor operable "for setting a transmit bit in an outgoing packet to a network." Claim 37 recites that the network device is operable to start the timer **when this transmit bit is set in the outgoing packet**. This outgoing packet is transmitted to another device on the network which reads the transmit bit and sets a receive bit in the next outgoing packet directed to the network device. See, e.g., Specification, p. 4, l. 23 – p. 5, l. 2. Upon receiving the packet, the processor stops the timer **when the receive bit is read**. In this manner, the timer reflects the network delay between the network device and the other device. Specification, p. 5, l. 2. Specifically, claim 37 requires a timer, and a processor operable for setting a transmit bit in an outgoing packet to a network and starting the timer **when the transmit bit is set** and for reading a receive bit in a received packet from the network and stopping the timer **when the receive bit is read**.

The Patent Office alleges that the timer of claim 37 is disclosed in Andersson, column 5, line 60 through column 6, line 60 and that the processor is disclosed in column 13, lines 29

through 45 of Andersson. Office Action of January 7, 2010, p. 3. Andersson, column 5, line 60 through column 6, line 60 discloses that the ICA bus adapter (referred to sometimes as "BA" in Andersson) utilizes an "Interval Timer Enable" bit in the BA sense and control register. Andersson col. 5, ll. 66-67. This "Interval Timer Enable" bit in this register allows for interval timer traps to be set or prevents them from being set. Andersson col. 5, ll. 65-68. Interval timer traps are *pre-determined time out intervals* (called "time outs" in Andersson) set by the interrupts of Start/Stop commands from the ICA Start/Stop Line Control facility. Andersson, col. 13, ll.40-41; col. 14, ll. 12-15; col. 14, ll. 25-27; col. 14, ll. 34-40; col. 14, ll. 44-47; col. 15, l. 5 – col. 16, l. 1; col. 17, ll. 30-32. These Start/Stop Commands may request that certain commands be performed to transfer or receive data bytes and are associated with certain time-out conditions to determine if certain events related to the Start/Stop commands have occurred. *Id.* The CCA timer counts down these pre-determined time outs. Andersson col. 15, l. 5 – col. 16, l. 1. Thus, the system disclosed by Andersson is not stopping the CCA timer when a bit is read but instead stops the timer after a *pre-determined amount of time*. Andersson thus does not disclose that the "stopping of the timer when the receive bit is read," as required by claim 37.

For example, the READ command in Andersson sets a time out interval to check for received characters in "Read." Andersson, col. 14, ll. 48-50. Consequently, the time out interval for the READ command determines a time out interval to *check* for received characters after a pre-determined amount of time, and thus this interval time trap does not determine an amount of time between the transmissions of received characters. Andersson, col. 14, ll. 48-50. In other words, it is perfectly possible for the received characters to have been received prior to the end of the time out interval. The time out interval for the READ command would cause these received characters to be checked after reaching the time-out interval but the time-out interval is in no way timing the time delay of received characters. Similarly, the INHIBIT command resets the time out interval, if the system is allowing for unlimited time between received characters. Andersson, col. 14, ll. 51-52. Clearly then, the time out interval is not timing when these characters are received, but instead the time out interval is being reset since an unlimited amount of time is allowed for receiving characters. The CCA timer is thus being utilized to count down *pre-determined amounts of time* and is not measuring the time related to time delay for transmission and reception of data. Thus, the interval timer functions disclose in col. 5, l. 60 – col. 6, l. 60 of Andersson cannot disclose a processor of claim 37 because the CCA timer in

Andersson is being stopped when **a pre-determined amount of time** has been elapsed not **when a receive bit is read,** as required by claim 37.

In fact, Andersson expressly states that the interrupts in Andersson are not associated with the actual transmission or reception of bytes but instead are related to the *requests* for service from the ICC. Andersson states:

> The CCA activates an interrupt [including interval time traps] on the PIO-bus thus requesting service from the ICC under the following circumstances: (1) a request for a data byte (Transmit), i.e., the normal output request (NOR) (2) availability of a data byte (Receive), i.e., the normal input request (NIR), (3) a change of level on the DCE interface or *timeout* on the CCA timer, which indicates 'B-stat is available'." (Andersson, col. 13, ll. 55-64; emphasis added).

The interrupts are thus associated with a *requests* to transmit, a *request* to receive, and timeouts on the CCA timer associated with these and *requests* for service from the ICC. Consequently, the CCA timer is not being started or stopped by bits set or read in transmitted and received data bytes. The time outs counted down by the CCA timer are instead set by requests for service from CCA to the ICC. As a result, the CCA timer of Andersson does not disclose "setting a transmit bit **in an outgoing packet**" and "starting the timer **when the transmit bit is set**," as required by claim 37, because the pre-determined time-outs are not started by setting bits in the transmitted and received bytes but rather by conditions and events associated with *requests* for transmitting and receiving data bytes. Consequently, the CCA timer in Andersson does not disclose the feature of claim 37 of starting the timer "**when the transmit bit is set**."

However, the Patent Office continues to allege that the CCA timer of the CCA measures a time delay related to the transmission and reception of bytes. Office Action of January 7, 2010, p. 3, 5-6. The Patent Office alleges that Andersson, column 13, lines 29-45 discloses that "start/stop operations are performed based on transmit and receive bit within a byte" and that "stop bit in the received byte is read to stop the timer accordingly." Office Action of January 7, 2010, p. 3. Andersson col. 13, ll. 33-44 states:

> [I]n *asynchronous line control*, the Start/Stop Line Control Facility provides a link to the Common Communications Adapter (CCA) 11 at the front end of ICA. For Start/Stop operations, the CCAs serialize/deserialize a byte, buffer one data byte, control the attached data communications equipment (DCE) and sense DCE conditions, establish *transmit and receive bit timing*, perform interval timer functions in accordance with the ICC, *append Start and Stop bits* onto transmitted bytes, test each received byte for a valid Stop bit and for odd parity, remove Start and Stop bits from each byte received, test each byte received for an all zero

condition and indicate when a Break sequence is being received, and transmit a continuous zero bit pattern as a Break sequence. (Emphasis added).

The Patent Office characterizes this passage by alleging that "the reference in Andersson to 'establish bit transmit and receive bit timing' and 'append Start and Stop bits onto transmitted bytes' appear to refer to establishing bit timing for bits since the link to the CCA is an asynchronous line. Andersson, Col. 13, lines 29-35. In addition, it appears that the 'Start/Stop operations' are identifying starting and stopping points for each transmitted byte and/or for starting and stopping the CCA's data communications. Andersson, Col. 13, lines 27 through Col. 16." Office Action of January 7, 2010, p. 6. The Patent Office then concludes, without any explanation, that establishing transmit and receive bit timing means that the time between the starting and stopping points is being measured by the system in Andersson. Office Action of January 7, 2010, p. 3.

Appellant asserts that the Patent Offices characterization of the reference is incorrect. When Andersson discloses establishing transmit and receiving timing it appears to be referring to the system ordering when bytes are to be received and transmitted along the asynchronous line. This is suggested by the fact that microcode commands for the ICC may be chained for an asynchronous line control but not for synchronous line control. Andersson col. 10, l. 65 – col. 11, l. 7. As a result, chain microcode commands are set up to order when the transmission and reception of bytes are transferred on an asynchronous line. When the ICA Start/Stop Line Control Facility of Andersson appends start and stop bits onto transmitted bytes, or test each received byte for a valid stop bit or odd parity, the time interval between the start bit and the stop bit is not being measured but instead the timing of the transmission and reception of bytes is being determined by the order of the microcode commands. Consequently, establishing transmit and receive bit timing is not referring to measuring a time between a start bit and a stop bit and the system in Andersson is not "**starting the timer when the transmit bit is set**" or "**stopping the timer when a receive bit is read**," as required by claim 37.

Admittedly, Andersson is not clear by what exactly it means by establishing "transmit and receive bit timing." However, nothing in Andersson discloses that the establishing transmit and receive bit timing has anything to do with the starting and stopping of a timer as required by the processor of claim 37. Furthermore, the Patent Office has the burden of establishing a prima facie case of obviousness and thus the Examiner should not be allowed to cite to vague and

undefined language in Andersson and declare, without evidence, that this language discloses the required features of claim 37.

Finally, even if we assume that, as the Patent Office alleges, that the time between the start and the stop bit of a transmitted byte is somehow being measured by the system in Andersson, Andersson still does not disclose the required features of claim 37. The processor in claim 37 must be operable "for setting a transmit bit in an outgoing packet to a network and **starting the timer when the transmit bit is set.**" The Patent Office alleges that the "establish[ing] of transmit and receive bit timing" in Andersson means that "start/stop operations are performed based on transmit and receive bits within a byte." Office Action of January 7, 2010, p. 3. According to the Patent Office, these start and stop bits indicate "starting and stopping points" for each transmitted and/or received byte. Office Action of January 7, 2010, p. 6. Accordingly, the start and stop bits must be appended to the byte before the byte or bytes are received or transmitted in order for a device to be able to determine the "starting and stopping points" of transmission or reception.

Thus, even under the Patent Office's erroneous assumption that the system in Andersson measures the time between the start and stop bit during reception of a byte, Andersson fails to teach a processor operable "**starting the timer when the transmit bit is set**," as required by claim 37. Under the Examiner's erroneous assumptions, the timer would have to be started after the start bit has been appended to the byte both by a destination device during reception and a transmission device during transmission because neither could transmit or receive bytes without being able to determine the starting and stopping points of transmission or reception. Thus, at best, the destination device would start the timer when the start bit is *received* by the destination device after the start bit has been appended to the received byte by the CCA. Similarly, the timer would be started upon *transmission* of the start bit and not when the start bit is set. While the Patent Office's assertions regarding Andersson are erroneous, even under these assumptions, Andersson does not disclose "a processor operable for setting a transmit bit in an outgoing packet to a network and starting the timer **when the transmit bit is set** and for reading a receive bit in a received packet from the network and stopping the timer **when the receive bit is read**," as required by claim 37. Claim 37 is thus patentable over the cited references.

2. None of the Cited References Either Alone or in Combination Discloses the Processor Operable for Reading a Set Transmit Bit in a Received Packet and for Setting a Receive Bit in Another Outgoing Packet in Accordance with Claim 39

Andersson does not teach or suggest "reading a set transmit bit in the **received packet**" and "set[ting] a receive bit in **another outgoing packet** in response to reading the set transmit bit," as required by claim 39. In this manner, the network device operates to assist another device in timing a network delay between itself and the network device. See, e.g., Specification, p. 4, l. 23 – p. 5, l. 2. The Patent Office states that column 13, lines 48-column 14, line 5 and table 3 lines 45-55 of Andersson disclose the required features of claim 39 because, according to the Patent Office, "next frame consists of the next bit setting protocol." Office Action of January 7, 2010, p. 3. Column 13, lines 48 through column 14, line 5 of Andersson discusses the activation of an interrupt by the CCA. The passage cited by the Patent Office does not refer actual data bytes being transmitted or received along the asynchronous line but rather *requests* related to commands to the ICC for transmitting and receiving databytes. Andersson, col. 13, ll. 55-64. Consequently, nothing in the passage cited by the patent office teaches or suggests "reading a set transmit bit in the **received packet"** and "set[ting] a receive bit in **another outgoing packet** in response to reading the set transmit bit," as required by claim 39.

The Patent Office also cites Table 3 lines 45-55 of Andersson. Table 3, lines 45-55 of Andersson discusses a WRITE PUI command of the synchronous data link facility of Andersson's system. Andersson, col. 20, ll. 23-35. During synchronous data transmission, the WRITE PUI command is used transfer a frame of data. Andersson, col. 27, ll. 16-18 To accomplish this, the starting address of the first frame of data is received by the ICA along with a value, NSCUR, which is an increment that indicates the next data byte. Andersson, col. 26, ll. 5-25; col. 27, ll. 16-18, 23-24, 36-38. Consequently, Table 3, lines 45-55 in Andersson discusses the values for incrementing a memory address to determine the next frame of data to transfer. Again, the Patent Office is citing to subject matter which is unrelated to the manipulation of transmitted or received data bytes but instead is related to commands for transmitting data bytes. The Patent Office's citation in no way shows "reading a set transmit bit in the **received packet**" and "set[ting] a receive bit in **another outgoing packet** in response to reading the set transmit bit," as required by claim 39. As a result, Andersson does not teach the required features of claim 39 and thus, claim 39 is patentable over the cited references.

3. None of the Cited References Either Alone or in Combination Discloses Sending an Indication to a User When the Value in the Round Trip Register is Greater than a Predetermined Value in Accordance with Claim 42

Claim 42 is dependent on claim 41, which depends on claim 37, and recites that the processor is further operable for comparing "a value in the round trip data register to a predetermine value and **sending an indication to a user** when the value in the round trip data register is greater than the predetermined value." The Patent Office alleges that Hanson at column 10, lines 36-54 discloses this feature of claim 42. Office Action of January 7, 2010, p. 4. However, the citation simply discloses a system where access modules in a network decrease network traffic to a transit module based on a congestion level. Hanson, col. 10, ll. 44-46. Hanson does not disclose that a user is notified when the congestion level is reached. Accordingly, Hanson does not disclose the required features of claim 42.

4. None of the Cited References Either Alone or in Combination Discloses Transmitting and Receiving State Machines Operable to Start a Timer When a Transmit Bit is Set and Stop a Timer When a Receive Bit is Received in Accordance with Claim 43

Claim 43 is an independent claim that recites a network device for use in a network transmitting packets that includes:

> a transmitting state machine operable for setting a transmit bit in an outgoing packet and starting the timer **when the transmit bit is set**; and
>
> a receiving state machine operable for reading a receive bit in a received packet and stopping the timer **when the receive bit is read**.

The Patent Office relies on the same arguments discussed above for claim 37 to support the rejection. Office Action of January 7, 2010, p. 3. For the same reasons as discussed above for claim 37, Appellant submits that Andersson does not teach the required features of claim 43. Accordingly, claim 43 is patentable over the cited references.

5. None of the Cited References Either Alone or in Combination Discloses the Receiving State Machine Operable for Reading a Set Transmit Bit in a Received Packet and for Setting a Receive Bit in Another Outgoing Packet in Accordance with Claim 45

Claim 45 recites the device in accordance with claim 43 wherein:

the receiving state machine is further operable for reading a set transmit bit in the **received packet** and for setting a receive bit in **another outgoing packet** in response to reading the set transmit bit in the received packet.

The Patent Office relies on the same arguments discussed above for claim 39 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above for claim 39, Appellant submits that Andersson does not teach the required features of claim 45. Accordingly, claim 45 is patentable over the cited references.

6. None of the Cited References Either Alone or in Combination Discloses Sending an Indication to a User When the Value in the Round Trip Register is Greater than a Predetermined Value in Accordance with Claim 48

Claim 48 is dependent on claim 47, which depends on claim 43, and further comprises:

a processing means operable for comparing the value in the round trip data register to a predetermined value and **sending an indication to a user** when the value in the round trip data register is greater than the predetermined value.

The Patent Office relies on the same arguments discussed above for claim 42 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above for claim 42, Appellant submits that Andersson does not teach the required features of claim 42. Accordingly, claim 42 is patentable over the cited references.

7. None of the Cited References Either Alone or in Combination Discloses a Processor Operable for Constructing an Outgoing First Voice Packet to a Network For Setting a Transmit Bit in the Outgoing First Voice Packet and For Starting a Timer When the Transmit Bit is Set in Accordance with Claim 49

Claim 49 recites a system for timing the transmission of voice packets that includes:

a processor operable for constructing an outgoing first voice packet to a network for setting a transmit bit in the outgoing first voice packet to the network, and for starting the timer **when the transmit bit is set**, and for monitoring a delay time of the network.

The Patent Office relies on the same arguments discussed above for claim 37 to support the rejection. Office Action of January 7, 2010, p. 3. For the same reasons as discussed above in

the argument for claim 37, Appellant submits that Andersson does not teach the required features of claim 43. Accordingly, claim 49 is patentable over the cited references.

8. None of the Cited References Either Alone or in Combination Discloses a Processor Operable for Checking the Second Voice Packet to Determine if a Receive Bit is Set and Stopping the Timer if the Receive Bit is Set in Accordance with Claim 51

Claim 51 recites the system in accordance with Claim 50, which depends on claim 49, wherein:

> the interface is operable for receiving a second voice packet and the processor is operable for checking the second voice packet to determine if a receive bit is set and **stopping the timer if the receive bit is set**.

The Patent Office relies on the same arguments discussed above for claim 37 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above in the argument for claim 37, Appellant submits that Andersson does not teach the required features of claim 37. Accordingly, claim 51 is patentable over the cited references.

9. None of the Cited References Either Alone or in Combination Discloses Sending an Indication to a User When the Value in the Round Trip Register is Greater than a Predetermined Value in Accordance with Claim 53

Claim 53 recites the system in accordance with claim 52, which is dependent on claim 51 50, and 49, wherein:

> the processor is further operable for comparing the value in the round trip data register to a predetermined value and **sending an indication to a user** when the value in the round trip data register is greater than the predetermined value.

Claim 53 contains some similar limitations to claim 42. The Patent Office relies on the same arguments discussed above for claim 42 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above in the argument for claim 42, Appellant submits that Hanson does not teach the required features of claim 53. Accordingly, claim 53 is patentable over the cited references.

10. None of the Cited References Either Alone or in Combination Discloses a Processor Operable for Checking the Second Voice Packet to Determine if a Transmit Bit is Set and Setting a Receive bit in the Outgoing Third Voice Packet in Accordance with Claim 54

Claim 54 recites the system in accordance with Claim 49 wherein:

> the processor is further operable for **receiving a second voice packet** and **checking the second voice packet to determine if the transmit bit is set** and further operable for constructing an outgoing third voice packet and **setting a receive bit in the outgoing third voice packet if the transmit bit is set** in the received second voice packet.

The Patent Office alleges that:

> Hanson discloses voice packet transmission (Fig. 1, col. 1 lines 40-45; col. 4 lines 18-33). The sequence of second and third voice packets would inherently follows the sequence after the first voice packet transmission and acknowledgement reception for timing delay and therefore while not explicitly disclosed however would be inherent to one of ordinary skill in the art that a second and third voice packet transmission would be apparently follow after the first voice packet transmission. (Office Action of January 7, 2010, p. 5).

The passages in Hanson cited by the Patent Office do not even remotely teach or suggest the required features of claim 54. Column 1, lines 40-45 and column 4 lines 18-33 of Hanson refer to the transmission of voice packets in general. The simple fact that multiple voice packets may be transmitted by the system disclosed in Hanson does not teach or suggest a processor operable to check "the second voice packet to determine if the transmit bit is set" and set "a receive bit in the outgoing third voice packet if the transmit bit is set in the received second voice packet," as required by claim 54. These relationships are not disclosed by the transmission or reception of multiple voice packets alone. Furthermore, claim 54 includes features similar to those in claim 39. Thus, claim 54 is patentable over Andersson for the same reasons as stated above for claim 39. Accordingly, claim 54 is patentable over the cited references.

11. None of the Cited References Either Alone or in Combination Discloses a Processor for Starting a Timer When the Transmit Bit is Set and for Reading a Receive Bit in a Received Packet from the Network and Stopping the Timer when the Receive Bit is Read in Accordance with Claim 55

Claim 55 recites a network device that includes:

> a processor coupled to the interface, the processor operable for setting a transmit bit in an outgoing packet to the network and starting the timer **when the transmit bit is set**, and for reading a receive bit in a received packet from the network, and stopping the timer **when the receive bit is read**.

The Patent Office relies on the same arguments discussed above for claim 37 to support the rejection. Office Action of January 7, 2010, p. 3. For the same reasons as discussed above in the argument for claim 37, Appellant submits that Andersson does not teach the required features of claim 55. Accordingly, claim 55 is patentable over the cited references.

12. None of the Cited References Either Alone or in Combination Discloses the Processor Operable for Reading a Set Transmit Bit in a Received Packet and for Setting a Receive Bit in Another Outgoing Packet in Accordance with Claim 56

Claim 56 recites the network device in accordance with Claim 55 wherein:

> the processor is further operable for reading a set transmit bit in the **received packet** and setting a receive bit in another **outgoing packet** in response to reading the set transmit bit in the received packet.

Claim 56 contains some similar limitations to claim 39. The Patent Office relies on the same arguments discussed above for claim 39 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above in the argument for claim 39, Appellant submits that Andersson does not teach the required features of claim 56. Accordingly, claim 56 is patentable over the cited references.

13. None of the Cited References Either Alone or in Combination Discloses Sending an Indication to a User When the Value in the Round Trip Register is Greater than a Predetermined Value in Accordance with Claim 58

Claim 58 recites the network device in accordance with claim 37 further comprising:

> a round trip register operable for receiving a value from the timer;
>
> wherein the outgoing packet and the received packet are voice packets; and

wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value and **sending an indication to a user** when the value in the round trip data register is greater than the predetermined value.

Claim 48 contains some similar limitations to claim 42. The Patent Office relies on the same arguments discussed above for claim 42 to support the rejection. Office Action of January 7, 2010, p. 4. For the same reasons as discussed above in the argument for claim 42, Appellant submits that Andersson does not teach the required features of claim 58. Accordingly, claim 58 is patentable over the cited references.

14. Claims 38, 40, 41, 44, 46, 47, 50, 52, and 57 Are Patentable Over the Cited References

Claims 38, 40, and 41 stand or fall with claim 37. Claims 44, 46, and 47 stand or fall with claim 43. Claims 50 and 52 stand or fall with claim 49. Claim 57 stands or falls with claim 55. Claims 38, 40, 41, 44, 46, 47, 50, 52, and 57 were rejected under 35 U.S.C. §103(a), as being unpatentable in view of Andersson in view of Hanson. Appellant respectfully transverses. Claims 38, 40, 41, 44, 46, 47, 50, 52, and 57 all depend on either claims 37, 43, 49, or 55 which Appellant has demonstrated are patentable. Accordingly, claims 38, 40, 41, 44, 46, 47, 50, 52, and 57 are patentable over the cited references and Appellant respectfully requests that the Board reverse the Examiner's rejection of the claims under 35 U.S.C. §103(a).

E. Claims 37-56 Were Rejected On the Grounds of Non-Statutory Double Patenting

Claims 37-58 were rejected on the grounds of non-statutory double patenting under 35 U.S.C. §103(c) over various claims in U.S. Patent No. 6,751,198. Appellant is not requesting that the Board consider the non-statutory double patenting rejection of claims 37-58 under 35 U.S.C. §103(c). Appellant is prepared to present arguments traversing the non-statutory double patenting rejection of the claims or submit a properly filed terminal disclaimer when this rejection is the only remaining rejection of the claims.

F. Conclusion

As set forth above, the combination of Andersson and Hanson does not teach or suggest each and every feature of claims 37, 39, 42, 43, 45, 48, 49, 51, 53, 54, 55, 56, and 58. As such, the Patent Office has not established where all the features recited in claims 37, 39, 42, 43, 45,

48, 49, 51, 53, 54, 55, 56, and 58 are disclosed or suggested by the prior art. Moreover, claims 38, 40, 41, 44, 46, 47, 50, 52, and 57 depend on either claims 37, 43, 49, and 55 and thus are patentable. As such, Appellant requests that the Board reverse the Examiner's rejections and instruct the Examiner that pending claims 37-58 are patentable over Andersson in view of Hanson under 35 U.S.C. §103(a). Appellant is then prepared to present arguments to the Examiner either traversing the double patenting rejection under 35 U.S.C. §103(c) of claims 37-56 or submit a proper terminal disclaimer to overcome the double-patent rejection.

Respectfully submitted,

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Date: August 9, 2010
Attorney Docket: 7001-710A

(8) CLAIMS APPENDIX

1-36. (Cancelled).

37. A network device for use in a network transmitting packets, the device comprising:

a timer;

a processor operable for setting a transmit bit in an outgoing packet to a network and starting the timer when the transmit bit is set, and for reading a receive bit in a received packet from the network and stopping the timer when the receive bit is read, and for monitoring a delay time of the network.

38. The network device in accordance with Claim 37 further comprising:

an interface coupled to the processor, the interface operable for coupling the network device to the network and for transmitting the outgoing packet.

39. The network device in accordance with Claim 37 wherein the processor is further operable for reading a set transmit bit in the received packet and for setting a receive bit in another outgoing packet in response to reading the set transmit bit in the received packet.

40. The network device in accordance with Claim 37 wherein the outgoing packet and the received packet are voice packets.

41. The network device in accordance with Claim 37 further comprising:

a round trip register operable for receiving a value from the timer.

42. The network device in accordance with Claim 41 wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value and sending an indication to a user when the value in the round trip data register is greater than the predetermined value.

43. A device for use in a network transmitting packets, the device comprising:

a timer;

a transmitting state machine operable for setting a transmit bit in an outgoing packet and starting the timer when the transmit bit is set; and

a receiving state machine operable for reading a receive bit in a received packet and stopping the timer when the receive bit is read.

44. The device in accordance with Claim 43 further comprising:

an interface coupled to the transmitting state machine, the interface operable for coupling the device to the network and for transmitting the outgoing packet.

45. The device in accordance with Claim 43 wherein the receiving state machine is further operable for reading a set transmit bit in the received packet and for setting a receive bit in another outgoing packet in response to reading the set transmit bit in the received packet.

46. The device in accordance with Claim 43 wherein the outgoing packet and the received packet are voice packets.

47. The device in accordance with Claim 43 further comprising:

a round trip register operable for receiving a value from the timer.

48. The device in accordance with Claim 47 further comprising a processing means operable for comparing the value in the round trip data register to a predetermined value and sending an indication to a user when the value in the round trip data register is greater than the predetermined value.

49. A system for use in timing the transmission of voice packets through a network, the system comprising:

a timer;

a processor operable for constructing an outgoing first voice packet to a network, for setting a transmit bit in the outgoing first voice packet to the network, and for starting the timer when the transmit bit is set, and for monitoring a delay time of the network.

50. The system in accordance with Claim 49 further comprising:

an interface coupled to the processor, the interface operable for coupling the system to the network and for transmitting the outgoing first voice packet.

51. The system in accordance with Claim 50 wherein the interface is operable for receiving a second voice packet, and the processor is operable for checking the second voice packet to determine if a receive bit is set and stopping the timer if the receive bit is set.

52. The system in accordance with Claim 51 further comprising:

a round trip data register operable for receiving a value from the timer.

53. The system in accordance with Claim 52 wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value and sending an indication to a user when the value in the round trip data register is greater than the predetermined value.

54. The system in accordance with Claim 49 wherein the processor is further operable for receiving a second voice packet and checking the second voice packet to determine if the transmit bit is set, and further operable for constructing an outgoing third voice packet and setting a receive bit in the outgoing third voice packet if the transmit bit is set in the received second voice packet.

55. A network device for use in a network transmitting packets, the network device comprising:

a link for communicating with external devices over the network, the link comprising,

an interface operable for coupling the link to the network and for transmitting and receiving packets,

a timer, and

a processor coupled to the interface, the processor operable for setting a transmit bit in an outgoing packet to the network, and starting the timer when the transmit bit is

set, and for reading a receive bit in a received packet from the network, and stopping the timer when the receive bit is read, and for monitoring a delay time of the network.

56. The network device in accordance with Claim 55 wherein the processor is further operable for reading a set transmit bit in the received packet and setting a receive bit in another outgoing packet in response to reading the set transmit bit in the received packet.

57. The network device in accordance with Claim 56 wherein the outgoing packet, the another outgoing packet and the received packet are voice packets.

58. The network device in accordance with Claim 37 further comprising:

a round trip register operable for receiving a value from the timer;

wherein the outgoing packet and the received packet are voice packets; and

wherein the processor is further operable for comparing the value in the round trip data register to a predetermined value and sending an indication to a user when the value in the round trip data register is greater than the predetermined value.

(9) EVIDENCE APPENDIX

Appellant relies on no evidence, thus this appendix is not applicable.

(10) RELATED PROCEEDINGS APPENDIX

As there are no related proceedings, this appendix is not applicable.